

# Organic field-effect bipolar transistors

A. Dodabalapur, H. E. Katz, L. Torsi,<sup>a)</sup> and R. C. Haddon  
AT&T Bell Laboratories, Murray Hill, New Jersey 07974

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Organic field-effect transistors (FETs) which employ two carefully selected active materials can function as *n* channel, *p* channel, or both *n*- and *p*-channel devices. It is shown that under an appropriate set of bias conditions the channel current in FETs with  $\alpha$ -hexathienylene ( $\alpha$ -6T) and  $C_{60}$  active layers consist of electron and hole components that are injected from the source and drain contacts into the  $C_{60}$  and  $\alpha$ -6T layers, respectively. © 1996 American Institute of Physics. [S0003-6951(96)02108-3]

There have been several recent reports of transistors with organic or polymeric active layers.<sup>1-5</sup> Nearly all these transistors are field-effect transistors (FETs). One exception is the polymer grid triode,<sup>6</sup> which is analogous to the GaAs permeable base transistor. Organic FETs are generally *p*-channel devices with the highest mobilities in the range 0.01–0.1 cm<sup>2</sup>/V s,<sup>3,4,7</sup> obtained with active materials such as  $\alpha$ -hexathienylene (or  $\alpha$ -sexithiophene or  $\alpha$ -6T) and oligothiophene derivatives such as  $\alpha,\omega$  dihexyl hexathienylene (H6T).<sup>3</sup> With such materials, thin-film transistors with on/off current ratios in excess of 10<sup>6</sup> and switching speeds of  $\sim 10$   $\mu$ s have been demonstrated.<sup>4</sup> One of the observed characteristics of organic materials employed as active materials in transistors is that they appear to transport only one carrier type. Thus, attempts to achieve inversion in *p*-channel FET materials such as  $\alpha$ -6T have been unsuccessful. This also appears to be the case for the few organic materials such as  $C_{60}$  that form *n*-channel accumulation mode FETs.<sup>5,8</sup> The picture that emerges from this is that organic materials that have been successfully used as active materials in TFTs appear to transport only one carrier type efficiently at room temperature.<sup>9</sup> In a recent article we showed that by employing a heterostructure active layer consisting of two carefully chosen materials ( $\alpha$ -6T and  $C_{60}$ , for example), it is possible to achieve *n*- and *p*-channel operation in a single transistor.<sup>10</sup> This happens as a result of the ability to create one type of accumulation layer in each of the active materials. The energy levels of the highest occupied and lowest unoccupied molecular orbitals (HOMO and LUMO) of  $\alpha$ -6T and  $C_{60}$  are such that the HOMO of  $\alpha$ -6T is energetically lower for holes or positive charges than the HOMO of  $C_{60}$  while the LUMO of  $C_{60}$  is energetically lower for electrons or negative charges.<sup>11</sup> Thus, when the gate is positively biased, an accumulation layer of electrons is formed in  $C_{60}$  and when the gate is negatively biased an accumulation layer of holes is formed in the  $\alpha$ -6T layer. Similar effects have also been observed after substituting the  $\alpha$ -6T with H6T and the  $C_{60}$  with PTCDA, indicating that these effects are not unique to the  $\alpha$ -6T/ $C_{60}$  combination. In this letter, we analyze the operation of such heterostructure organic field-effect transistors and show that currents of both polarities can be simultaneously injected from the source and drain contacts. Such

transistors are dominantly *n* channel in some bias regimes and dominantly *p* channel in other regimes. More interestingly, in some bias conditions the electron and hole currents are approximately equal. It is, therefore, appropriate to refer to these devices as field-effect bipolar transistors. It may be possible to employ such transistors to make all-organic complementary circuits.

The schematic layer structure of such a transistor is shown in Fig. 1. The gate is an *n*-type Si wafer with an Au Ohmic contact. The gate dielectric is a 300 nm thick layer of thermally grown SiO<sub>2</sub>. Au contact pads are defined above the SiO<sub>2</sub> and form the source and drain Ohmic contacts. The organic layers are sublimed above the SiO<sub>2</sub> and contact pads and the source and drain are probed through these layers with sharp tungsten probes. As described in Ref. 10, an accumulation layer of holes or positive carriers is induced into the  $\alpha$ -6T layer adjacent to the SiO<sub>2</sub> when a negative gate-source voltage is applied and an accumulation layer of electrons or positive carriers is induced into the  $C_{60}$  layer when a sufficient positive bias is applied to the gate. When a source-drain bias is applied in addition to the gate bias, the induced charge profile gets significantly modified. Indeed, for positive  $V_{DS}$  and  $V_{GS}$  and with  $V_{DS} > V_{GS}$ , an accumulation layer of holes is formed near the drain in  $\alpha$ -6T and an accumulation layer of electrons is formed near the source in  $C_{60}$ , as illustrated in Fig. 1. The reason this happens is that for  $V_{DS} > V_{GS}$ , the gate is effectively negatively biased with respect to the drain

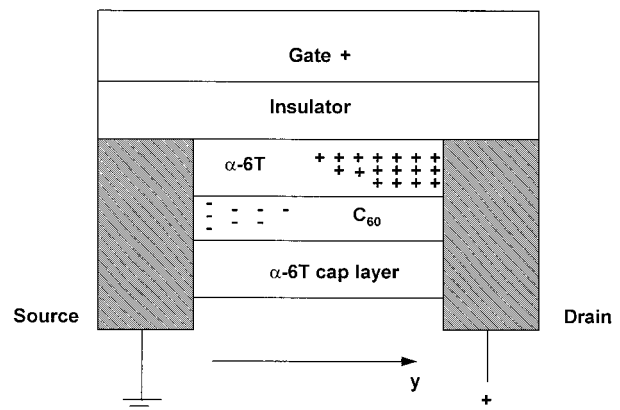


FIG. 1. Schematic layer structure of the organic heterostructure field-effect transistors used in this study. Also depicted is the field-induced charge profile under positive gate-source ( $V_{GS}$ ) and drain-source voltages ( $V_{DS}$ ) such with  $V_{DS} > V_{GS}$ . It may be noticed that for a given value of  $y$  only one charge type is present.

<sup>a)</sup>On leave of absence from the Department of Chemistry, University of Bari, Bari, Italy.

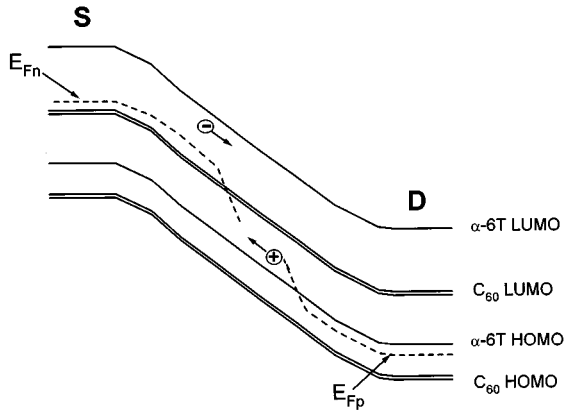


FIG. 2. Schematic energy band diagram under the same bias conditions shown in Fig. 1.

at/near the drain contact leading to an accumulation of holes. The schematic energy band diagram corresponding to this case is shown in Fig. 2. The effective field-induced charge is a function of lateral position in the channel and for positive gate-source ( $V_{GS}$ ) and drain-source ( $V_{DS}$ ) is given by

$$n_{\text{ind}}(y) = -\frac{\epsilon_i}{qd_i} \{ (v_{GS} - v_{T_n}) - [v(y) - v_{T_p}] \}, \quad (1)$$

where  $\epsilon_i$  and  $d_i$  are the insulator dielectric constant and thickness,  $q$  is the elementary charge, and  $V_{T_n}$  and  $V_{T_p}$  are the threshold voltages for the  $n$ - and  $p$ -channel modes of operation. This total effective charge is separated into the electron and hole components and integrated with respect to voltage to obtain expressions for the source or drain current. The electron currents have familiar forms in the linear and saturation regions.<sup>12</sup> The hole current has a different form since the charge density also depends on  $V_D$ , and for small  $V_{GS}$  and  $V_{TP}$  is approximately given by:  $I_D(p) \propto V_{DS}^2$ , provided  $|V_{DS}| > |V_{GS}|$ .

Figures 3(a) and 3(b) show the drain current characteristics of an  $L=4 \mu\text{m}$  FET with positive gate-source ( $V_{GS}$ ) and drain-source ( $V_{DS}$ ) biases. These are typical bias conditions for  $n$ -channel operation. However, for low  $V_{DS}$  we see unusual behavior with the drain current ( $I_D$ ) increasing supralinearly with  $V_{DS}$ . The magnitude of this current, however, falls with increasing  $V_{GS}$ , until it reaches a minimum for  $V_{GS}=30$  and  $40$  V, beyond which the drain current increases with increasing  $V_{GS}$ , as it should for normal  $n$ -channel operation. The currents observed at low values of  $V_{GS}$  (and only when  $V_{DS} > V_{GS}$ ) are hole currents and are a result of an accumulation layer of holes which is induced near the drain contact when  $V_{DS} - V_{T_p} > V_{GS}$  (depicted in Fig. 2). Since  $V_{T_p} \sim 0$  V, we expect to see a significant  $I_D$  when  $V_{DS} > V_{GS}$ . This is exactly what is seen in Fig. 3(b) for  $V_{GS}=0, 10$ , and  $20$  V. This evidence for hole current flow is particularly clear in the  $\alpha$ -6T/ $C_{60}$  material system since [see inset in Fig. 3(a)]  $n$ -channel  $C_{60}$  FETs have a large threshold voltage due to electron traps. This enables us to observe the behavior of the hole current more clearly without much interference from electron currents for a significant range of  $V_{DS}$  and  $V_{GS}$ . The field effect mobilities of electrons extracted from Fig. 3(a) is  $0.005 \text{ cm}^2/\text{V s}$ . Higher mobilities

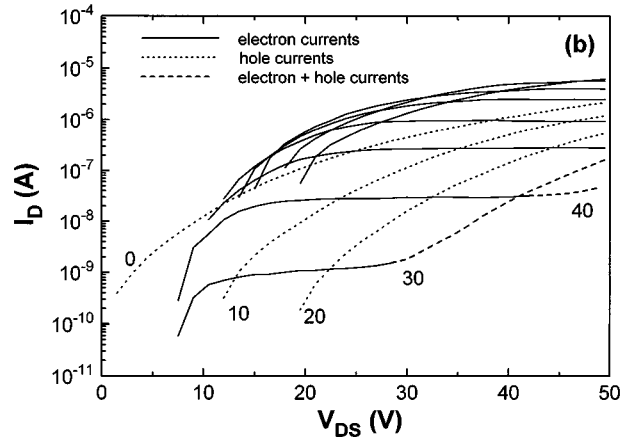
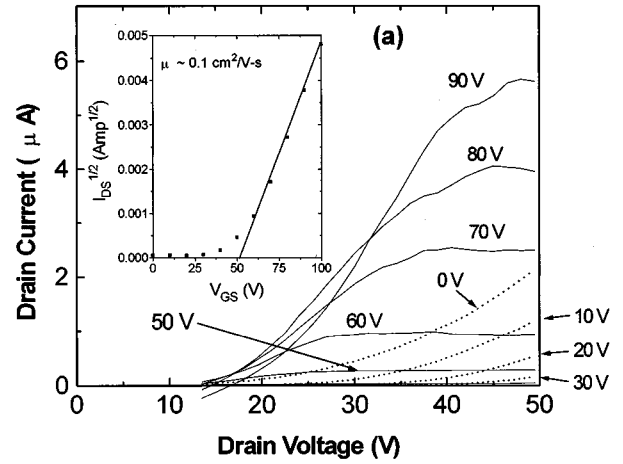


FIG. 3. (a) Drain current ( $I_D$ ) of an  $\alpha$ -6T/ $C_{60}$  FET as a function of positive drain source voltages for different gate voltages. The curve for  $V_G=40$  V is not labeled. In the inset is plotted the square root of  $I_D$  for a  $C_{60}$  FET (without an  $\alpha$ -6T active layer) as a function of the gate voltage. The large threshold voltage of the  $C_{60}$  FET is a result of electron traps. (b) Drain current  $I_D$ , as a function of positive  $V_{DS}$  plotted on a semilogarithmic scale for different gate voltages.

have been obtained in  $C_{60}$  FETs without the  $\alpha$ -6T active layers ( $\sim 0.1 \text{ cm}^2/\text{V s}$ ). This can be seen in the inset in Fig. 3(a) and has been discussed in Ref. 8.

As  $V_{GS}$  starts to approach the threshold voltage of the  $n$ -channel part of the device, we start to observe well-behaved electron currents with linear and saturation regions. This is seen in Figs. 3(a) and 3(b) for  $V_{GS} > 30$  V. This regime is dominantly  $n$  channel in which the electron currents exceed the hole currents. For  $V_{GS}=30$  and  $40$  V, we see something very interesting. The drain current exhibits the typical  $n$  channel linear and saturation behavior for low  $V_{DS}$  but abruptly increases for  $V_{DS} > V_{GS}$ . At this point, the electron current injected from the source (and which flows in the  $C_{60}$  layer) is augmented by an increasing hole current which flows in the  $\alpha$ -6T layer. Indeed, for a particular set of bias conditions, the electron current injected from the source is exactly equal to the hole current injected from the drain. These bias points occur close to the inflections in the 30 and 40 V curves. Although these currents low in separate but adjacent layers, the Coulomb attraction may cause the electrons and holes to recombine making this a true gated bipolar device.

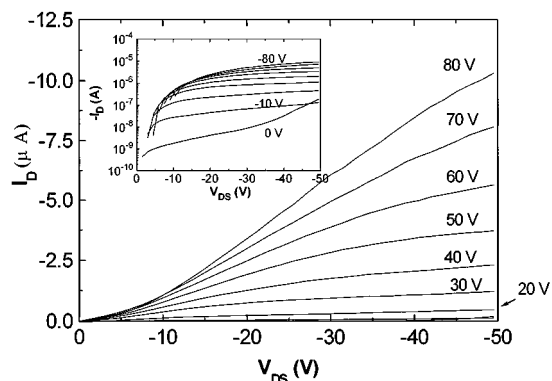


FIG. 4. Drain current as a function of negative drain source voltages for a series of negative gate voltages (dominantly  $p$ -channel regime). In the inset are shown the same data plotted on a semilogarithmic scale.

In Fig. 4, are shown the current-voltage characteristics of the FET when operated in the dominantly  $p$ -channel mode. The gate-source and drain-source voltages are negative. Nearly all the currents in the bias regimes depicted in Fig. 4 are hole currents. This is because of the large threshold voltage for  $n$ -channel operation. Most of the electrons induced near the drain when  $|V_{DS}| > |V_{GS}|$  are trapped and do not contribute to current flow. This is so until  $|V_{DS}| - V_{T_n} > |V_{GS}|$  when electron currents are measurable. This is seen in the inset in Fig. 4 for  $V_{GS} = 0$  where  $I_D$  starts to increase nonlinearly beyond  $|V_{DS}| = 35$  V. This point corresponds to the voltage required to result in significant electron currents in the  $n$ -channel mode of operation, as can be deduced from the inset of Fig. 3(a). The availability of dominantly  $n$ - and  $p$ -channel behavior from the same device will simplify the fabrication of complementary circuits based on this technology. It would be possible to fabricate circuits without having to pattern the organic materials. This is an important consideration since many organic materials are quite sensitive to processing environments. Complementary circuits in which a single transistor can function as either an  $n$ - or  $p$ -channel device have been proposed and analyzed by Neudeck *et al.*, for  $a$ -Si based FETs.<sup>13</sup> They take advantage of the two-

carrier transport that can occur in  $a$ -Si. What we have done here is to create a very similar situation, but with two active materials, each of which transports only one carrier type. It is necessary to use two active materials because most organic materials which have been used so far as active materials in field-effect transistors transport only one carrier type.<sup>14</sup>

In summary, we have shown that organic heterostructure field-effect transistors with a carefully selected pair of active materials exhibit both  $n$ - and  $p$ -channel operation. The chief criteria involved in the selection of the materials are the in-plane transport properties and heterojunction energy level offsets. Under certain bias conditions, the channel current consists of both electron and hole components injected from the source and drain into the two active materials. In other bias conditions these FETs are unipolar being either  $n$ - or  $p$ -channel depending on the sign of the gate voltage.

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