Prof. Jaydeep Kulkarni [3] and Prof. Sanjay Banerjee [4] are co-principal investigators on a new National Science Foundation (NSF) grant to explore the advancement of energy efficient design in integrated circuits.

With the rapid advances in computing systems spanning from billions of IoT (Internet of Things) devices to high performance exa-scale supercomputers, energy efficient design is an absolute must. In a modern System-on-a chip (SoC) design, supply voltage scaling is the primary driver to reduce the energy consumption. Voltage droops caused by the peak switching current as well sudden changes in current activity of various logic blocks requires larger voltage guard-bands, thereby degrading the system level energy efficiency. Thus, there is a critical need to develop circuit topologies to reduce the peak switching currents as well as sudden current fluctuations to reduce the voltage droops and to realize a compact and energy-efficient power delivery network.

This research envisions a novel soft-switching transistor architecture named as Soft-FET for realizing energy-efficient CMOS circuits. The targeted efficient operations can be realized by utilizing abrupt phase change behavior in transition metal oxides such as Vanadium Dioxide and Niobium dioxide. The team plans to fabricate and demonstrate phase transition material based Soft-FET integrated circuit prototypes by heterogeneous integration with baseline silicon technology. Various Soft-FET architecture circuit blocks such as digital logic, memory arrays, and power management units will be investigated to realize energy efficient integrated circuits. Principles underlying the research in this project can be readily transferred to existing SoC designs benefiting the integrated circuit design industry, and ultimately the consumer society. The students engaged in this research will be trained in device fabrication, integrated circuit, test-chip design, and heterogeneous system integration issues, thus contributing to the much needed workforce development in chip design industry.

Links
[3] https://www.ece.utexas.edu/people/faculty/jaydeep-kulkarni
[4] https://www.ece.utexas.edu/people/faculty/sanjay-banerjee